NR

Code No: A5711

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, March/April-2011
MODELING AND SYSTHESIS WITH VERILOG HDL
(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

\- - -

1. Explain the synthesis process in both verilog and VHDL languages with suitable block diagrams. [12]

2. a) How are blocking assignments different from non-blocking assignments?
   b) Write verilog HDL code for decade counter using structural modeling. [12]

3. Explain in details the different features of verilog language. [12]

4. a) Draw the logic circuit and explain how a Variable is synthesized as a latch.
   b) Give an example to show that variable GRADE is not a latch, when it is assigned a value in all branches of the IF statement. [12]

5. a) What are the four kinds of loop statements in Verilog HDL? Give examples.
   b) Write a sample program to explain about the function of de assign statement. [12]

6. Draw the block schematic of a Mealy finite state machine. Using reg variable, model the state of the machine. [12]

7. a) Differences between verilog & VHDL languages.
   b) Explain the systhesis of compiler directives. [12]

8. Write notes on:
   a) Synthesis of edge Triggered Flip Flops
   b) Synthesis of three state buffers. [12]

* * * * * *